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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Response to Arguments

Applicant's arguments filed with respect to claims 13, 15-29, 31-40, 43-50, and 52-54 on have been fully considered but they are not persuasive.

The Applicant presents seven arguments contending the Examiner's pending rejection of claims 13, 15-29, 31-40, 43-50, 52-54 under 35 U.S.C. 103(a) as being unpatentable over Eifrig et al., (hereinafter referred to as "Eifrig") in view of Pian et al., (hereinafter referred to as "Pian"). However, after a careful consideration of the arguments presented and further scrutiny of the applied references, the Examiner must respectfully disagree and maintain the grounds of rejection for the reasons that follow.

Firstly, after summarizing the salient features of claims 13, 44, 53 with the relevant portions the applied primary reference (Request for Reconsideration: page 2, lines 8-22;page 3, lines 18-30), and parsing over the Examiner's rationale regarding the obviousness of "separation" (Request for Reconsideration: page 2, lines 22-25: page 3, lines 1-3), the Applicant argues that the secondary reference Pian fails to provide support for "separate processors" as in the claims, because, according to the Applicant, the preprocessor and the encoder are not separate processors, but are just shown to be separate elements (Request for Reconsideration: page 3, lines 4-17 and 31-32; page 4, lines 1-2). The Examiner respectfully disagrees. First, one notes that the pre-processor is indeed separate from the compressor, because it can be bypassed completely (i.e. "excluded) from the normal operation of the disclosed encoder (Pian: column 4, lines 1-4). Therefore, since it is not integral to the operation of the encoder, it is clearly separate. Now, we come to the whether the both the pre-processor and the encoder are

both processing entities. The Examiner notes that by inherency, the label "preprocessor" explicitly encompasses a processing function. Lastly, we turn to Pian to characterize the processing capabilities of the compression system. In particular, the reference clearly notes that the preprocessor provides or formats the signal for easier processing by the compression system (Pian: column 4, lines 4-10). Therefore, the Examiner maintains that when analyzed as such, Pian clearly discloses the use of “separate processors” in a manner that would make obvious the incorporation of the doctrine of separation that has been staunchly established as unpatentable by the Courts, *Nerwin v. Erlichman, 168 USPQ 177, 179, (PTO Bd. of Int. 1969).*

Secondly, the Applicant argues that the secondary reference Pian fails to provide support for "packetizing and then storing in memory" as in the claims (Request for Reconsideration: page 4, lines 3-17 and similarly for claims 44 and 53, pages 5-6). The Examiner respectfully disagrees. It is noted that the BSP of Eifrig allows for packing and unpacking of the video data (Eifrig: column 4, lines 1-4). However, packing (i.e. packetizing) would only occur when outputting from the encoder (Eifrig: column 4, lines 30-35). That means that the unpacking (i.e operative on already formed packets) occurs when the information is input into the BSP from the parser/demux element. The formation of packets is a resultant output of the parser/demux element so that the BSP can “unpack” the packets and execute conventional transcoding. The Examiner further notes that the available co-processor memory reads on the memory of the claims since it accounts for storage of data between co-processors such as the VLIW processor and

the BSP (Eifrig: column 6, lines 35-40). Accordingly, the Examiner maintains that the combination of references meets the limitations.

In response to applicant's argument that the references fail to show certain features of applicant's invention (Request for Reconsideration: page 4, lines 18-30), it is noted that the features upon which applicant relies (i.e., "one or more applications performed by software") are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).*

With regard to claim 29 and applicants' argument that: "The Office fails to establish how Eifrig discloses a memory controller and a sequencer (much less that they couple two processors) and thus the Office fails to meet its burden of establishing a primafacie case of obviousness with respect to claim 29.". The examiner respectfully disagrees and wants to point out that because the DMA engine (col. 9, ln. 5-13) handles all movement of media data between data cache and external RAM concurrently with VLIW processor execution and thus is considered both as memory controller and sequencer.

Having answered all of the applicants' arguments, the examiner maintains all of his rejections.

/Nhon T Diep/

Primary Examiner, Art Unit 2621